

WHAT WE CLAIMED ARE:

1. A power MOSFET device with reduced snap-back and being capable of increasing avalanche-breakdown current endurance, which has sequentially a drain with N<sup>+</sup> silicon substrate, an N<sup>-</sup> epitaxial layer formed on said N<sup>+</sup> silicon substrate, a source contact region formed of N<sup>+</sup> doped well and P<sup>+</sup> doped well implanted after etching in a P<sup>-</sup> well formed on said N<sup>-</sup> epitaxial layer, and a gate electrode with deposition of polysilicon above a channel region between said N<sup>-</sup> epitaxial layer and N<sup>+</sup> source contact region, said device is characterized in that: Said source contact region is formed by etching into said P<sup>-</sup> well first and implanting P<sup>+</sup> dopant to the interface between said N<sup>-</sup> epitaxial layer and P<sup>-</sup> well, and the source contact region of said N<sup>+</sup> well and that of said P<sup>+</sup> well are not at the same level, by which it is possible to increase the avalanche-breakdown current durable capability of the power MOSFET device.
2. A method of manufacturing a power MOSFET device with reduced snap-back and being capable increasing avalanche-breakdown current endurance, comprising the following steps:
  1. An N<sup>-</sup> epitaxial layer is epitaxially grown on a N<sup>+</sup> silicon substrate;
  2. A field oxide is grown on said N<sup>-</sup> epitaxial layer;
  3. Etching said field oxide and growing a gate oxide layer;
  4. Depositing a polysilicon layer;

5. Performing photo masking and etching said polysilicon layer to form a polysilicon gate, and implanting and driving-in P<sup>-</sup> dopant to form a P<sup>-</sup> well;
6. Applying photo mask of N<sup>+</sup> dopant and implanting N<sup>+</sup> dopant to form a N<sup>+</sup> source;
7. Producing a photoresist, and after the source region is etched, implanting P<sup>+</sup> dopant to form a P<sup>+</sup> well, and subsequently removing the photoresist;
8. Depositing BPSG (Boro-Phospho Silicate Glass); and
9. Performing a metalization of said source contact and processing the back contact of wafer to form a drain contact.

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